CprE 558 Project Proposal

Inverted Pendulum

# Group Members

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# Preface

We are completing this project for CprE 558 and CprE 583. Both classes will involve the inverted pendulum but each class will be concerned with different aspects. This document describes aspects relevant to CprE 558.

Below is breakdown of which group member is in which class.

CprE 558:

* Matthew Cauwels
* Kyle Fischer
* Eric Middleton

CprE 583:

* Matthew Cauwels
* Eric Middleton

# Project Type

This is an implementation based project.

# Project Goal

In this project, we will be comparing the settling time, steady-state error, and peak-overshoot values for the Quanser Inverted Pendulum (IP) Cart using the same LQR controller on various platforms: the Quanser VoltPAQ-X1 & G8-USB DAQ using Matlab/Simulink (Quanser implementation), a Xilinx Zybo board with the controller implemented directly on the FPGA (FPGA implementation), a Xilinx Zybo board running FreeRTOS using an RMS scheduler (RMS implementation), and a Xilinx Zybo board running FreeRTOS using an EDF scheduler (EDF implementation).

A Xilinx Zybo board with an LQR controller implemented in hardware will be implemented for the CprE 583 portion of the lab. If this implementation is successful, it will also be compared to the implementations described above, but the work done for CprE 558 will not be dependent upon the work done for CprE 583.

# Approach

We will first develop a linearized model of our inverted pendulum system. This will provide a set of constant matrices that will be used in the LQR controller. Using the same constants across all implementations, we will measure the settling time, steady-state error, and peak-overshoot of each implementation. In order to make the computation more intensive, and hopefully see a more dramatic difference between implementations, more states may be added to the controller. The addition of these states won’t effect the computations mathematically but they will affect the instructions executed by the processor. The states used will be consistent across all implemenations.

# Expected Outcomes

We expect to see the following hierarchy (ranked best to worst) for each measured value:

1. Hardware implementation
2. FPGA implementation
3. RMS implementation
4. EDF implementation
5. Quanser implementation

# References

[1] Apkarian, Lacheray, Martin (2012). Student Workbook IP02 Base Unit Experiment for Matlab/Simulink Users.

[2] Quanser (2012). User Manual IP02 Base Unit Experiment – Setup and Configuration

[3] N. Safari-Shad, “Modern Control Systems – EE4310 Lab Project #4”, University of Wisconsin-Platteville, Platteville, WI, 2017, pp.1-3

[4] P. Zhang, A. Mills, J. Zambreno and P. Jones, “The Design and Integration of a Software Configurable and Parallelized Coprocessor Architecture for LQR Control”, *Journal of Parallel and Distributed Computing (JPDC)*, 2017.